Digital Design Lab

Spring 2026

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Digital Design LAB

Spring 2026

Outline

Week 1	General Announcement and Lab Administration
Week 2	Lab 0: Use of Lab equipment
Week 3	Lab 1: Characteristics of Logic Gates
Week 4	Lab 2: Logic Pen
Week 5	Lab 3: Modified Linear Decoder
Week 6	Lab 4: FPGA Combinational Circuits (1)
Week 7	Lab 4: FPGA Combinational Circuits (2)
Week 8	Lab 5: Multivibrator Circuits
Week 9	Midterm Exam (No Class)
Week 10	Lab 6: Simple Traffic Controller (1)
Week 11	Lab 6: Simple Traffic Controller (2)
Week 12	Lab 7: Serial Data Transmissions (1)
Week 13	Lab 7: Serial Data Transmissions (2)
Week 14	Lab 8: FPGA Sequential Circuits (1)
Week 15	Instructor on Leave (No Class)
Week 16	Lab 8: FPGA Sequential Circuits (2)
Week 17	Final Exam

Component list

NE555
74LS00
74LS02
74LS04
74LS07
74LS08
74LS32
74LS47
74LS74
74LS76
74LS86
74LS90
74LS93
74LS123
74LS138
74LS153
74LS163
74LS164
74LS165
CD 4011
HEX SW
Button SW
7-Segment
LED (R,G,Y)
BNC
Buzzer (5v)
Clip Wire
Bread Board
VR 10k
VR 50k
VR 100k
R: 100, 200, 470, 1 k, 3 k, 10 k
C: 100 μF, 0.1, 0.01, 0.001

LAB 0: Use of Lab Equipment

Objective

- To understand the usage of lab equipment, including oscilloscope, function generator, and power supply
- To be familiar with the wiring with the **breadboard**

Background knowledge

1. Find out the reference manuals of the oscilloscope, power supply, and function generator
2. Learn how to set up the oscilloscope in X-Y mode. You may find many useful information over the Internet and on the appendices of this manual

Experiments, observations, and discussion

Experiment 1: Using DC Power Supply

1. **Connect the circuit of Fig. 1. Make sure you understand how to use the breadboard correctly. You can find additional information on the appendix of this manual or over the Internet.**
2. Turn on power supply.
3. Set the output of the power supply to DC +4V.
4. Use the circuit shown in Fig. 1 to check whether DC voltage actually appears at the two output terminals of the power supply.
5. Read out the consumed current of the circuit. The current is ___ mA. **Can you get the current reading from the power supply directly?**
6. If we need to have 10 mA of current through the diode, the power supply should be set to _____ Volts.

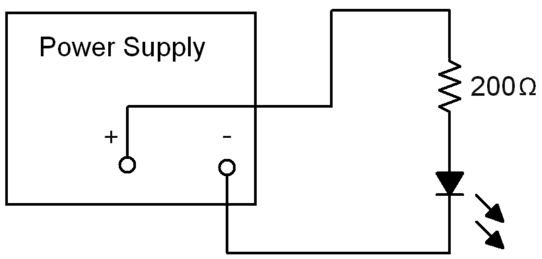


Fig. 1. LED circuit for power supply.

Experiment 2: Using Function Generator and Oscilloscope

1. Turn on the function generator (FG) and the oscilloscope (scope).
2. Set the FG to generate 10 kHz, $1V_{pp}$ sine wave. **Remember to get signals from the output, but not sync, BNC jack**.
3. Connect the output of the FG to CH 1 input of the scope.
4. Observe the waveform shown on the screen of the scope.
5. Does the displayed wave have the correct amplitude and frequency? **If the readings of the FG are not correct, change the load impedance from 50 Ω to high impedance. (Learn how to do it by yourself)**
6. Obtain a copy of the screen shot of the scope.
7. Include the screen-shot picture in your report.

Experiment 3: Pulse Generation

1. Turn on the function generator (FG) and the oscilloscope (scope).
2. Set the FG to generate 1 kHz, $5V_{pp}$ rectangular wave.
3. Use the **"high/low level"** function in the FG so that the waveform is from 0 volt to 5 volts.
4. Use the "duty" function to adjust the duty cycle of the square wave to 25 %.
5. Set the coupling mode of the scope to "DC" coupling.
6. Connect the output of the FG to CH 1 input of the scope.
7. Observe the waveform shown on the screen of the scope.
8. Ask the instructor to check your screen.
9. Obtain a copy of the screen shot of the scope, and include the screen shot in your report.

Experiment 4: Oscilloscope in X-Y Mode

1. Connect the circuit shown in Fig. 2.
2. Set the oscilloscope to X-Y mode and observe the curve.
3. Slowly increase or decrease the frequency of the sine wave.
4. Can you see any change of the pattern (known as the Lissajous pattern) on the oscilloscope screen? Describe your observation results.
5. Ask the instructor to check your screen.
6. Include the screen-shot picture of the scope in your report.

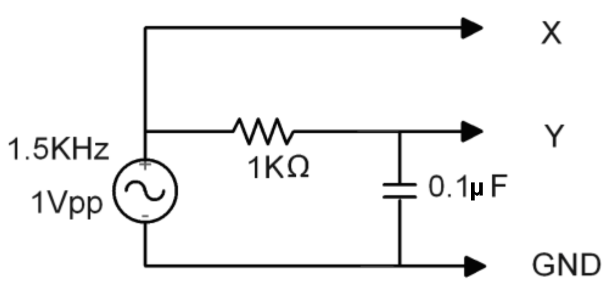


Fig. 2. R-C circuit to show the Lissajous pattern.

LAB 1: Characteristics of Logic Gates

■ Objective

- To understand the DC & AC characteristics of TTL and COMS gate
- To know how to measure TTL and CMOS parameters with an oscilloscope

■ Background knowledge

1. Study the definition of t_{PHL} and t_{PLH}
2. Find the I_{IL}, I_{IH}, V_{OL}, and V_{OH} of 7404 gates in the datasheet
3. **Clearly explain the differences between power, ground, input, and output of an 74LS04 gate**

■ Experiments, observations, and discussion:

Experiment 1: Propagation Delay of 74-series Gates

1. Connect 5 **inverters** as shown in Fig. 1. **Don't forget to connect the power and ground from the power supply to any IC used in all of the experiments in this semester.** According to the datasheet, the IC is 74LS___. Its Vcc is pin ___ and GND is pin ____. **All 74 series ICs use a power of 5 Volts.**
2. Properly set the output of the FG to generate 5 Vpp **(0 V to 5 V)**, 100 kHz pulses with a duty cycle of 25 %.
3. Use CH 1 and CH 2 in the scope to measure the average propagation delay of the five gates, and then calculate the average delay per gate. The delay per gate is t_p = ______.
4. Include a screen shot of the scope in your report.

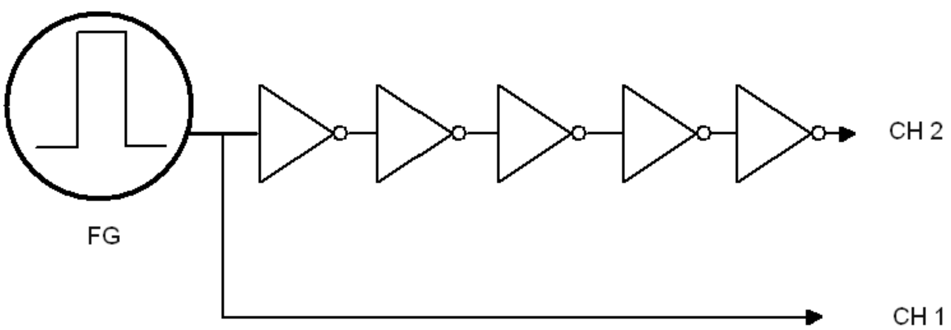


Fig. 1. Circuit to measure the propagation delay of a gate.

Experiment 2: Ring Oscillator (74 series)

1. Connect 5 inverters as shown in Fig. 2. No input is necessary. That is, the FG is not used here. **Remember the FG is not used to provide power to the ICs.**

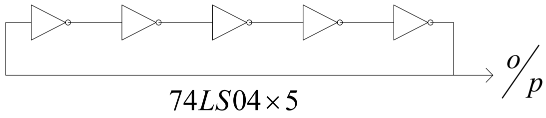


Fig. 2. Ring oscillator.

2. Observe the waveform at the output **(o/p)** using the scope and measure the period of the displayed waveform.
3. Ask the instructor to check your screen.
4. Based on the waveform, the average propagation delay for an inverter is t_P = ______ns. **Explain how to calculate this value.**
5. Include a screen shot of the scope in your report.
6. Is the measured delay in this experiment consistent with that in Experiment 1? If not, why not?
7. If the sixth inverter is added to the circuit, what will happen? What will happen if the seventh is added? Explain why.
8. If your circuit has more than one IC, remember to give power to all ICs in the circuit.

Experiment 3: Ring Oscillator (40 series)

1. This experiment shows the differences between gates of the 74-series and those of 40-series.
2. Connect the circuit shown in Fig. 3.

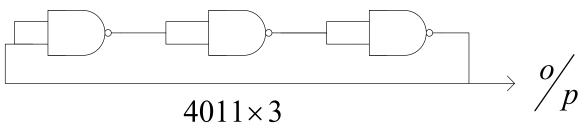


Fig. 3. Ring oscillator using 4000 series.

3. Set V_{DD} of the IC to +5V.
4. Calculate the propagation time for the gate. The delay time is ___ ns.
5. Set V_{DD} to +10V and +15V, respectively, and calculate the propagation time again. The delay time is ___ ns for 10 V and ___ ns for 15 V.
6. What is the relation between the propagation time and the supply voltage for a 40 series gate? Among the 74-series gates and 40-series gates, which series generally has a faster speed? Why?
7. Include a screen shot of the scope in your report.

Experiment 4: Transfer Characteristics (74 series)

1. Connect the circuit shown in Fig. 4. Use 74LS04 as the NOT gate.
2. Set the FG to generate $5V_{pp}$ **(0 V to 5 V)** triangular wave as the input to the gate.
3. Use the X-Y mode to plot the transfer characteristics of the gate.
4. **Adjust the oscilloscope knobs so that the origin of the transfer curve is on the center of the screen**.
5. Based on the transfer characteristics, when the input voltage is ____ V, the output of the gate changes its state **(midpoint** from high to low).
6. Ask the instructor to check your screen.
7. Include a screen shot of the scope in your report.

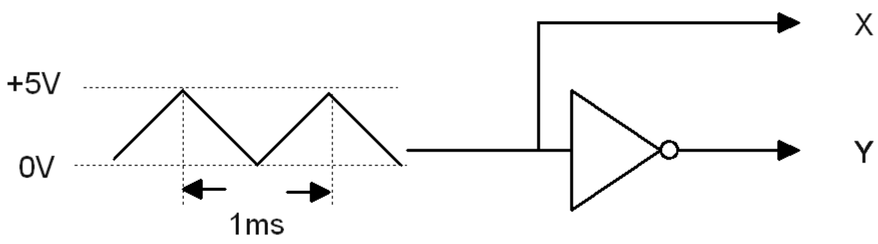


Fig. 4. Circuit to measure the transfer characteristics of a TTL gate.

LAB 2: Logic Pen

■ Objective

- ➢ To understand how to read datasheet
- ➢ To learn how to construct a logic probe based on simple components

■ Background knowledge

1. You need to study the pinouts of 74LS00 before the lab begins
2. Find the pinout of the 7-segment display used in the lab. If necessary, use a multi-meter to confirm your findings
3. The 7-segment display contains 7 LEDs in one package, as shown in Fig. 1. Note how the segments are named (a, b,c, etc.). The equivalent circuit of a Common-Anode (C/A) 7-segment display is shown in in Fig. 2. It has a common point connecting all of the anode terminals of the LEDs. This common point should connect to V_{CC} (i.e., +5V).

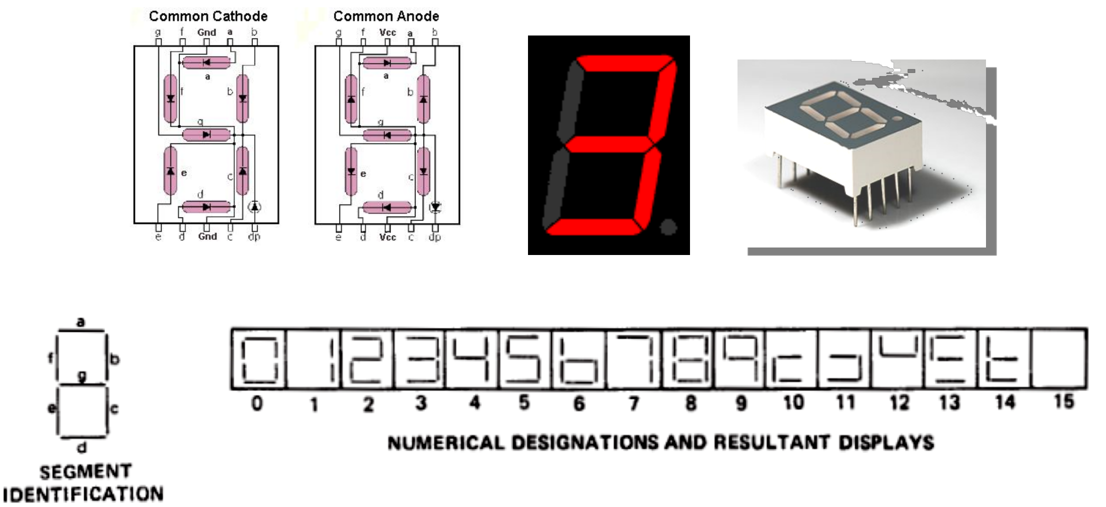


Fig. 1. Designation and display setup

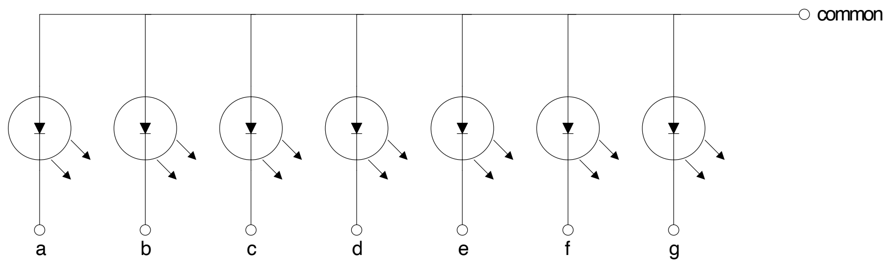


Fig. 2. The equivalent circuit of a seven-segment display

■ Experiments, observations, and discussion:

Project Part 1

1. Fig. 3 is the schematic diagram of a simple logic pen to indicate the voltage status (H/L) of a point. The IC used in the diagram is 74LS00.
2. Build either the circuit given in Fig. 3 or the circuit you design, and then ask the instructor to check your worked circuit. The 150 Ω resistor may be replaced by 330 Ω or even 470 Ω.
3. In the report, you need to analyze the circuit you implement and explain why the circuit works.

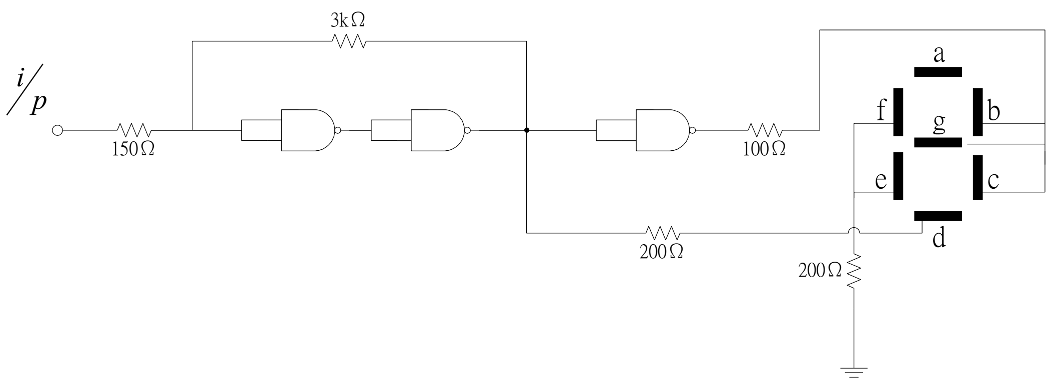


Fig. 3. Schematic diagram of a logic pen.

4. For your reference, the equivalent circuit of a 7-segment display is given in Fig. 2. This type of 7-segment is called Common-Anode (C/A) as it has a common point connecting all of the anode terminals of the LEDs. This common point should connect to V_{CC} (i.e., +5V).

Project Part 2

1. Based on the given design, modify the circuit to show 0 and 1 with the additional switch to choose between positive logic and negative logic. For positive logic, high means logic 1, whereas in negative logic, high means logic 0. **In short, your circuit has to have a input line and a switch**.
2. The mode switch must be accomplished by a DIP switch with one end tied to ground, as shown below.
3. **Why do we connect the switch as shown in Fig. 4. Can we exchange the positions of resistor and switch? What is the adverse effect of doing that? Recall that we use 74xx TTL gates, whose input currents are not symmetric in High and Low states.**

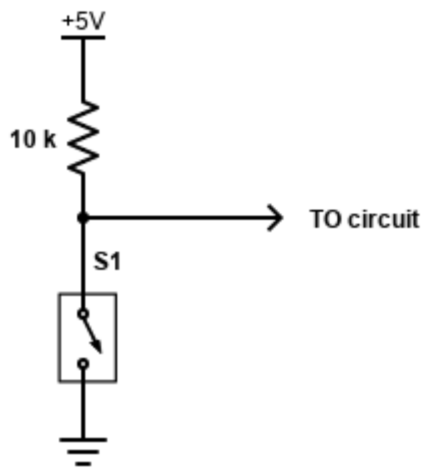


Fig. 4. Proper way of connecting a switch.

LAB 3: Modified Linear Decoder

Objective

- To understand the design procedure of a combinational circuit
- To be familiar with the use of MSI chips

■ Background knowledge

1. Review the basics of decoders and find out the chip number of a decoder
2. Design your circuit prior to entering the lab.

■ Experiments, observations, and discussion:

Project description

1. In this lab, you are asked to design a modified linear decoder, where only two LEDs are light at a time.
2. Fig. 1 is the block diagram of the entire circuit. The input to the decoder is a HEX encoding switch, and the output of the decoder connects to 7 LEDs or an LED array. If the input is $0 \le n \le 5$ (binary coded using b_0 to b_2 of the DIP switch), then the LEDs numbered (n+1) and (n+2) are light. For example, if n = 5, then number 6 and number 7 LEDs should be illuminated.
3. Ask the instructor to check your worked circuit. Also prepare a copy of your schematics with you, as the instructor may need to review it.
4. You need to describe the design procedure along with the schematic diagram in the report.

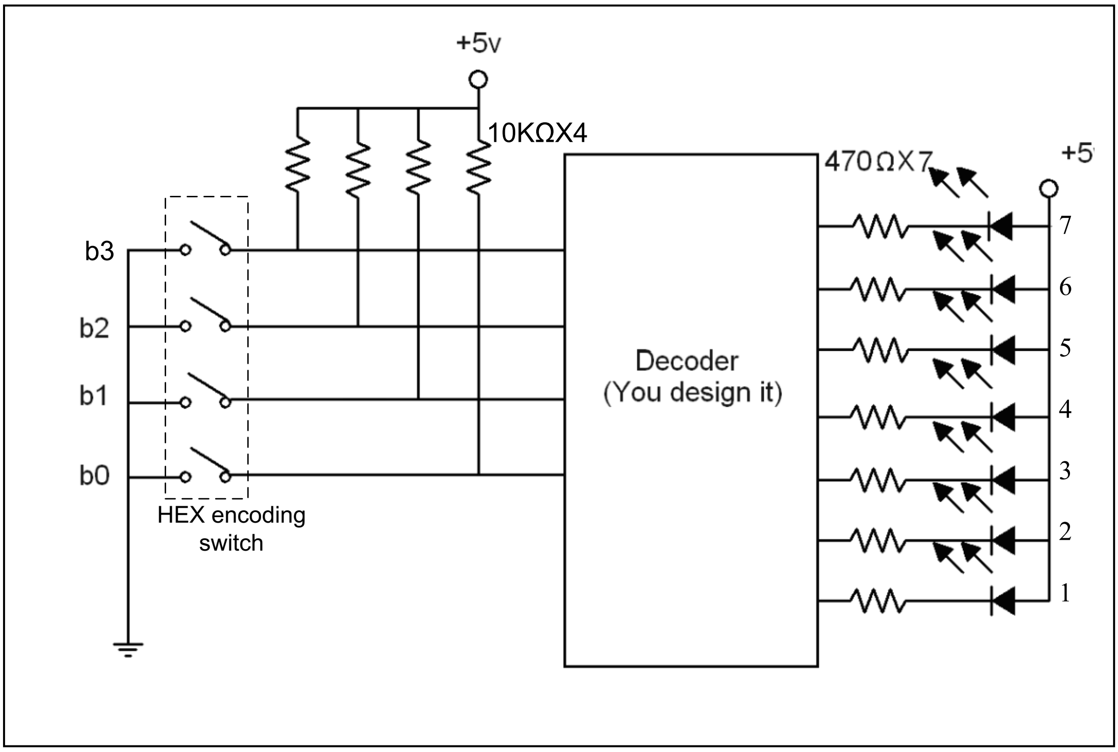


Fig. 1. Block diagram of a modified linear decoder.

LAB 4: FPGA Combinational Circuits

■ Objective

- ➢ To be familiar with the VHDL codes
- ➢ To know how to use the FPGA board for circuit design

■ Background knowledge

1. Read the VHDL chapters in the textbook
2. Read the provided ppt file to know how to use the Quartus Lite and FPGA board

■ Experiments, observations, and discussion:

Project Part 1

1. FPGAs are widely used in industry nowadays. They are flexible and easy to use. This lab shows how easy it could be if you know the basic steps to program an FPGA via VHDL.
2. In the project, you need to build an 8-bit priority encoder. A priority encoder produces a value of n if the input binary number is $00\ldots0b_n\text{xx}\ldots\text{xx}$, where x represents "don't care" and $b = 1$. For example, the encoded output for binary numbers from 00100000 to 00111111 is five. **In case the binary is 00000000, then the display is not illuminated**.
3. The input bits are set by switches SW[7] to SW[0], where **SW[7] is the MSB.** The encoded result is shown on 7-segment display **HEX0**.
4. You need to read the user's manual of the FPGA board to know the pin assignments of the switches and the 7-segment display. Note that the displays are of common anode type. Thus, you need to use a low-level voltage to light a segment.

Project Part 2

1. Design a 4-bit by 4-bit unsigned multiplier and show the results (less than 100_{10}) on two 7-segment displays in decimal format.
2. **Again, you must use SW[7] to SW[4] and SW[3] to SW[0] as the binary inputs and the results are shown on HEX0 and HEX1.**

LAB 5: Multivibrator Circuits

■ Objective

- ➢ To be familiar with multivibrator circuits
- ➢ To know how to use the 555 and 74LS123 chips to construct astable and monostable multivibrator circuits

■ Background knowledge

1. Read the data sheet of NE555 and 74LS123
2. Find the meanings of astable multivibrator and monostable multivibrator (one shot)
3. Figure out the differences between retriggerable and non-retriggerable one-shots

■ Experiments, observations, and discussion:

Experiment 1: Astable Multivibrator

1. Build an astable multivibrator to generate 10 kHz square wave using NE555. Use +5V to power NE555.
2. Consult the available documents over the Internet to figure out **how to make the duty cycle of the wave to be 50 %**.
3. Ask the instructor to check your worked circuit.
4. Include the screen-shot picture of the scope and your schematics in the report.

Experiment 2: Monostable Multivibrator

1. Build a monostable multivibrator (one shot) using IC 74LS123 to generate pulses with width T = 10 μs, as shown in Fig. 4.1.
2. Connect the FG to your circuit to verify if your circuit is correct. The input pulses have a duty cycle of 50%.
3. Include the screen-shot picture of the scope and your calculation steps in your report.

Fig. 4.1. Verification for one-shot circuit.

Experiment 3: 555 One-Shot

1. Repeat Exp 2, but use NE555 instead of 74LS123.
2. What do you observe at the output (i.e., Q) of the one-shot?
3. Is there any difference at the output waveforms obtained using 555 and 74LS123 as the one-shot? Why? Hint: **555 is not an edge triggered device**.
4. Use whatever method (found over the Internet) to make the output waveform the same as that from 74LS123. In your design, you can add additional circuit containing diodes, transistors, capacitors, and resistors at the input side of the 555. But you cannot add any circuit at the output of the 555.
5. Ask the instructor to check your worked circuit.

LAB 6: Simple Traffic Controller

■ Objective

- ➢ To know how to design sequential circuits with counters
- ➢ To know how to use counter & decoder chips

■ Background knowledge

1. Review the data sheets of 74xx90 and 74xx93.
2. Review the astable multivibrator circuit again

■ Experiments, observations, and discussion:

Project Description

You will design and implement a simple traffic controller in this project. The controller controls two sets of traffic lights, the East-West bound (E-W) lights and the **North**-South bound (N-S) lights. Each set of lights, as you may see one in a street, contains three lights, namely, Red (R), Green (G), and Yellow (Y). The main function of the controller is to turn on/off lights in a logical manner as follows:

E - W	R	R	R	R	R	G	G	G	G	Y
N - S	G	G	G	G	Y	R	R	R	R	R

Repeat

Project Part 1

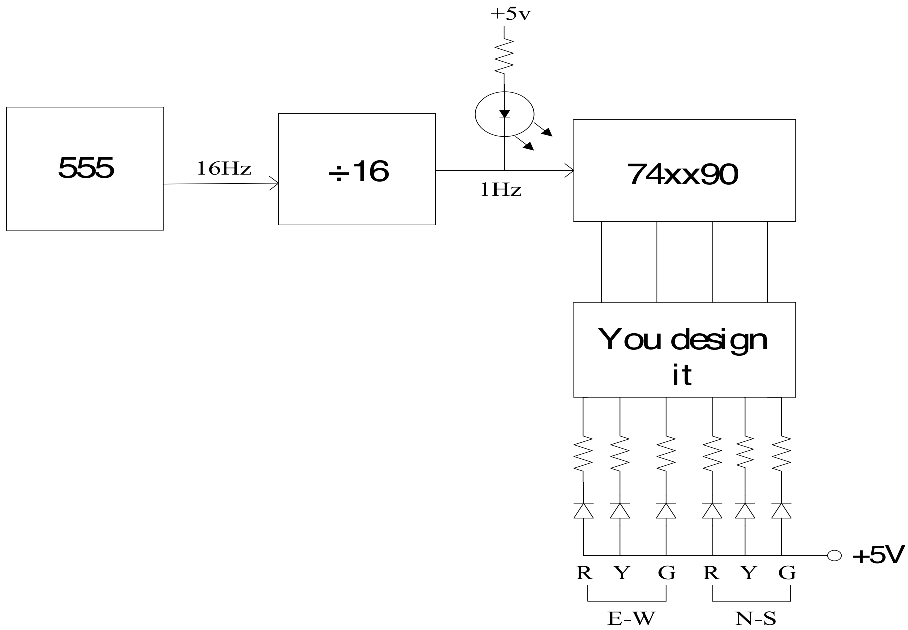
1. For part I, you need to design a combinational circuit to decode a BCD number to turn on or off corresponding LEDs. The truth table is given below.

	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001
R1	✓	✓	✓	✓	✓					
Y1										✓
G1						✓	✓	✓	✓	
R2						✓	✓	✓	✓	✓
Y2					✓					
G2	✓	✓	✓	✓						

2. Ask the instructor to check your worked circuit.

Project Part II

1. Complete the traffic controller circuit, as shown below.
2. The number of states in this project is 10. Therefore, a divide-by-10 counter is an essential part of your circuit.
3. Ask the instructor to check your worked circuit.
4. You may use whatever ICs, but you have to buy them if you intend to use any ICs not given in the lab.



LAB 7: Serial Data Transmissions

■ Objective

- ➢ To learn how to design a serial communication circuits
- ➢ To learn how to write VHDL programs to implement sequential circuits

■ Background knowledge

1. Read *Fundamentals of Logic Design* to refresh the knowledge of sequential circuit design using VHDL
2. Review the procedure of sequential circuit design
3. Read data sheets of **74LS164, 74LS165, and 74LS166**

■ Experiments, observations, and discussion

Project Part 1

1. This project is to build a data communications system. The system has a transmitter part (TX) and a receiver part (RX). The data are serially sent from TX to RX. To simplify the problem, the clock is also sent to RX. Therefore, data, clock, and ground lines are required for data transmission.
2. The first part of the project is to build TX. A block diagram for this part is shown in Fig. 1. To transmit data, the user needs to set the HEX encoding switches to represent 7 bits of the data. After that, the user pushes the "transmit" button for the **7-bit data** to be sent.
3. The waveform of the data line is given in Fig. 2. The line is normally at high level. When data are to be transmitted, the line goes low for one clock period (called start bit), and then the data bits are serially sent from bit 0 to 6 with high level representing 1 and low level representing 0.
4. To serially send out data bits, you may use a **parallel-to-serial** (P/S) converter.
5. **To simplify the design, you may supply the clock pulses to your circuit by using a function generator. The frequency of the clock is set to 100 Hz.**
6. **As the frequency of the clock is high, you need to produce a narrow pulse for loading data bits when pushing the button**
7. After completing this part of circuit, you need to use the scope to catch the waveform of the data line, and then ask the instructor to check the waveform and the circuit. You also need to include the waveform (screen shot) in the report.

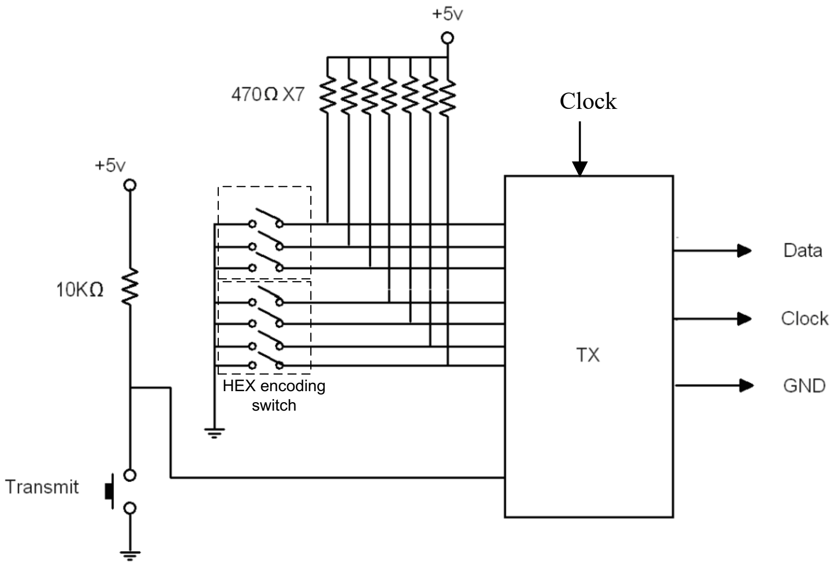


Fig. 1. The transmitter part of a data communications system.

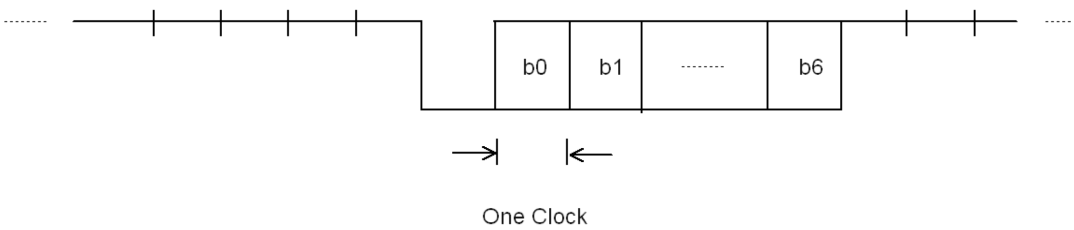


Fig. 2. The waveform of the data line.

Project Part 2

1. This part is to build the receiver (RX). The receiver should have two seven-segment displays to show the received data bits, one display for the most significant three bits, and the other one for the rest four bits. The received data should be latched until next 7-bits are available. The block diagram of the complete system is shown in Fig. 3.
2. You may also use a serial-to-parallel shift register for serial to parallel conversion.
3. Ask the instructor to check your worked circuit.
4. You need to describe the design procedures of both parts in the report.

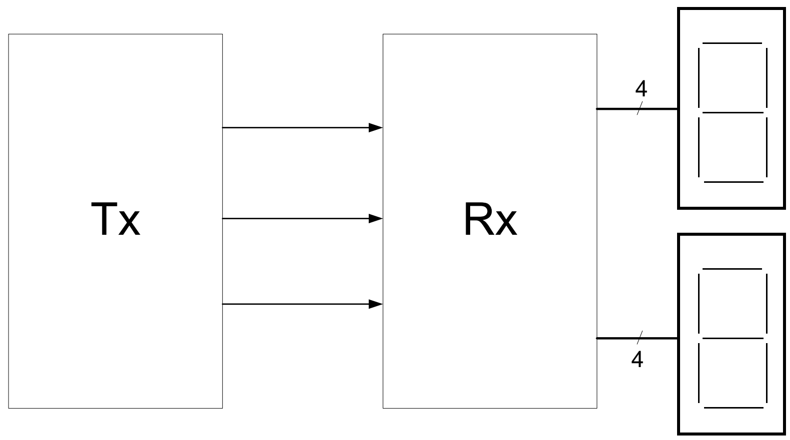


Fig. 3 Block diagram of the complete system.

LAB 8: FPGA Sequential Circuits

■ Objective

- ➢ To learn how to write VHDL programs to implement sequential circuits
- ➢ To learn how to debug a moderately complicated VHDL program

■ Background knowledge

1. Read *Fundamentals of Logic Design* to refresh the knowledge of sequential circuit design using VHDL

■ Experiments, observations, and discussion

Project Part 1

1. In the project you will build a simple traffic model using the FPGA board. The model has two sets of traffic lights (with each set having Red, Yellow, and Green LEDs). The R-G-Y cycle has 10 units, where the Red light lasts 5 units, Yellow 1 unit, and Green 4 units.
2. One unit in the R-G-Y cycle is set to

   t_{unit} = 1 + 0.25 * (group number)   (sec).

   For example, group 8 must design a counter to have a time unit of

   1 + 0.25 * 8 = **3** second

5. Present a copy of your program when checking off.

Project Part 2

1. Include two counters to show the remaining time of red lights in the unit of seconds. You can ignore any fractional second and show only whole seconds.

Appendix

1. 驗收紀錄
2. 報告封面範例
3. 報告內容範例
4. **Background information (Thanks to Prof. KWK)**
    - **Breadboard**
    - **Power supply**
    - **Function generator**
    - **Oscilloscope**
    - **Introduction to logic family, static characteristics, and comparisons**

LAB 0: Use of Lab Equipment

Group no.: ________________

Students' names: ________________

Experiment 3: Pulse Generation

Instructor's signature: ________________

Experiment 4: Oscilloscope in X-Y Mode

Instructor's signature: ________________

LAB 1: Characteristics of Logic Gates

Group no.: ________________

Students' names: ________________

Experiment 2: Ring Oscillator

Instructor's signature: ________________

Experiment 4: Transfer Characteristics

Instructor's signature: ________________

LAB 2: Logic Pen

Group no.: ________________

Students' names: ________________

Part I

Instructor's signature: ________________

Part II

Instructor's signature: ________________

LAB 3: Modified Linear Decoder

Group no.: ________________

Students' names: ________________

Instructor's signature: ________________

LAB 4: FPGA Combinational Circuits

Group no.: ________________

Students' names: ________________

Part I

Instructor's signature: ________________

Part II

Instructor's signature: ________________

LAB 5: Multivibrator Circuits

Group no.: ________________

Students' names: ________________

Experiment 1: Astable Multivibrator

Instructor's signature: ________________

Experiment 3: 555 One-Shot

Instructor's signature: ________________

LAB 6: Simple Traffic Controller

Group no.: ________________

Students' names: ________________

Part I

Instructor's signature: ________________

Part II

Instructor's signature: ________________

LAB 7: Serial Data Communications

Group no.: _______________

Students' names: _______________

Part I

Instructor's signature: _______________

Part II

Instructor's signature: _______________

LAB 8: FPGA Sequential Circuits

Group no.: ________________

Students' names: ________________

Part I

Instructor's signature: ________________

Part II

Instructor's signature: ________________

國立台北科技大學
資訊工程系

數位邏輯設計實習報告

Lab 0: Use of Lab Equipment

（報告封面範例）

第？組： (學號)

(姓名)

(學號)

(姓名)

（報告內容範例）

LAB 1: Characteristics of Logic Gates

Background knowledge

t_{PHL} 的定義為 ...

t_{PLH} 的定義為 ...

7400 的 fan-in 之定義為 ...

7400 的 fan-out 之定義為 ...

Experiment 1: Ring Oscillator (74 series)

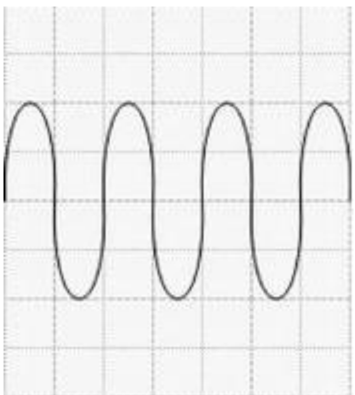
連接電路後之波形如下：

(波形)

t_p 的數值為 ...

Experiment 2: Ring Oscillator (74 series)

連接 5 個 NOT 後之波形如下 :(僅供參考，請用實際量測之結果取代)



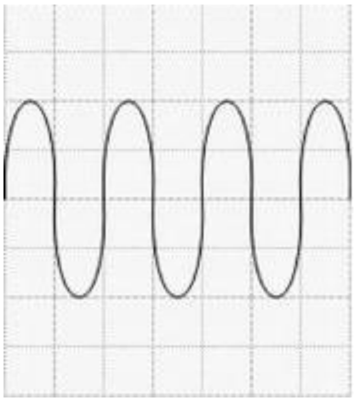
週期為 … 因此平均 propagation delay 為 … (公式 …)

此數值與實驗一相比，相對較大(小)，因為 …

第六個 NOT 加入後，…，因為 …

Experiment 3: Ring Oscillator (40 series)

連接 3 個 NAND 後之波形如下(V_{DD} = +5 V)：(僅供參考，請用實際量測之結果取代)



因此邏輯閘的 propagation time 為 …
當 V_{DD} 為 +10V 時 propagation time 為 …
當 V_{DD} 為 +15V 時 propagation time 為 …
對於此次實驗所得到的 V_{DD} 與 propagation time 之關係為 …
由這次的實驗中，可以觀察到 74 系列和 40 系列的不同為 …(請討論速度，propagation time 等方面問題)

Experiment 4: Transfer Characteristics

連接電路後之波形如下：

(波形)

LAB 6: Simple Traffic Controller

Background knowledge

74LS90 的接腳為 …
74LS93 的接腳為 …

Design Procedure

需求：

…

過程：（設計技巧）

(Truth table)
(Minimization)
⋮
(Boolean algebra)
⋮
(Circuit)

結果：

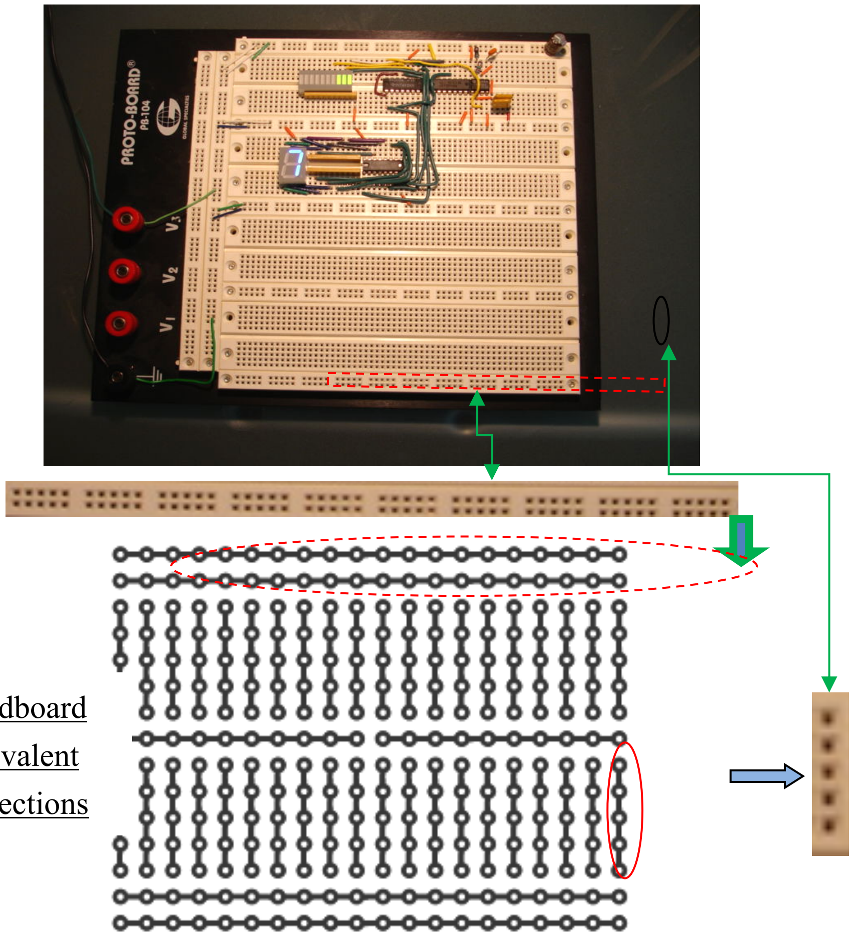
（說明你們的電路合乎需求，可以附加圖片證明）

討論：

（你們的心得：遇到的問題、解決問題的方法、技巧…等）

Background info

- **The *breadboard (麵包板)***



Breadboard equivalent connections

➢ Feeding and measurement cables: power code, BNC cable

- **DC Power Supply (Agilent E3620A)**

Dual output DC PS: 0 ~ 25V at 1A.

➢ **PS Front panel**

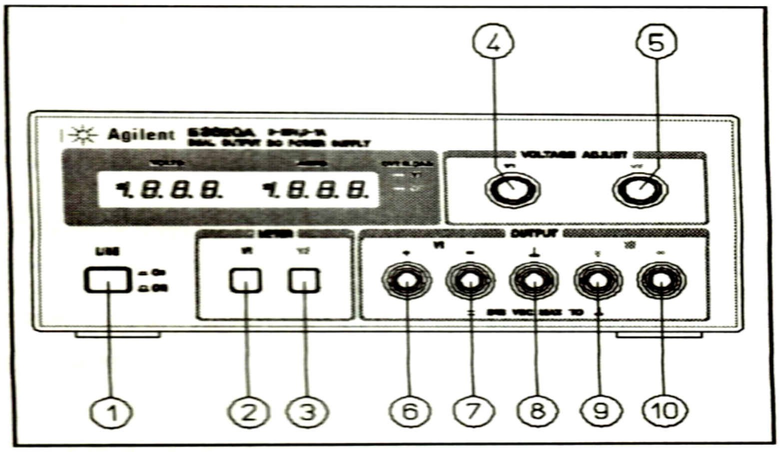


Figure 2. Front-Panel Controls and Indicators

1 ~ Power switch
2 and 3 ~ Voltage and current meter selection button
4 and 5 ~ voltage control (set voltage level)
6 and 7 ~ +V1 and –V1 output terminal (第一組電壓輸出)
8 ~ Chassis grounding (共同接地接點)
9 and 10 ~ +V2 and –V2 output terminal (第二組電壓輸出)

➢ **<u>Understanding various configurations of a PS</u> (Fig. 5.2 ~ 5.5)**

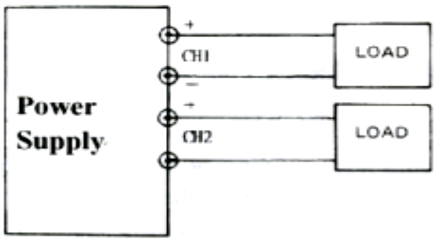


Fig. 5-2 Independent Operation

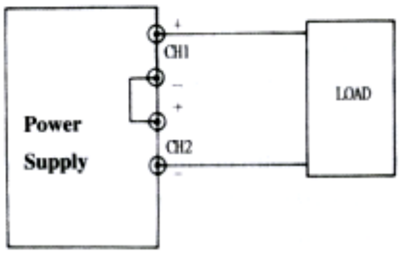


Fig. 5-3 Single Supply

Series operation

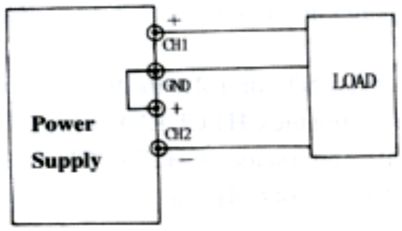


Fig. 5-4 Positive and Negative Supply

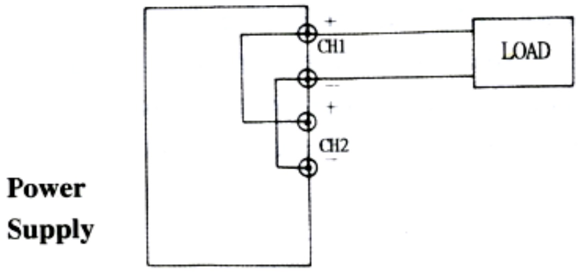
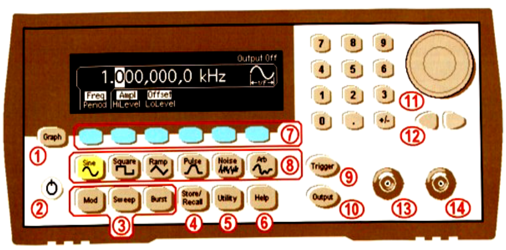


Fig. 5-5 Parallel Tracking Operation

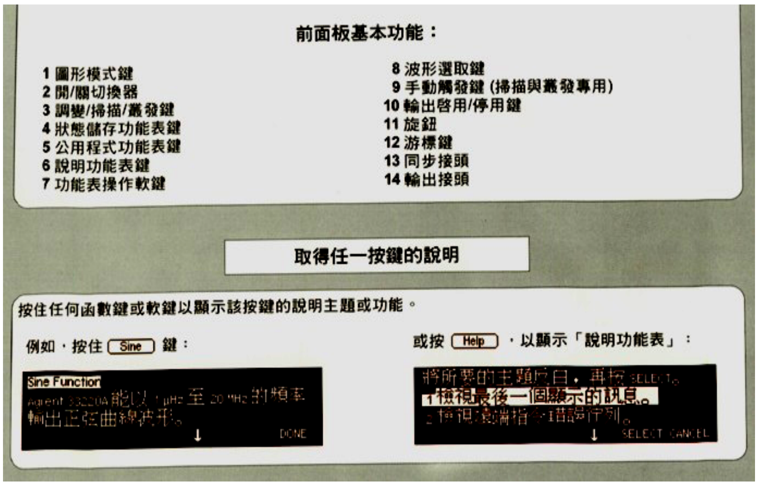
- **<u>Function Generator (Agilent 33220A)</u>**

  Agilent 33220A (20MHz, Function/Arbitrary waveform Generator)

  ➢ **<u>Front Panel</u>**



發亮的按鍵表示作用中的按鍵及函數 (例如上方的 Sine)。


前面板基本功能：

1 圖形模式鍵
2 開/關切換器
3 調變/掃描/叢發鍵
4 狀態儲存功能表鍵
5 公用程式功能表鍵
6 說明功能表鍵
7 功能表操作軟鍵
8 波形選取鍵
9 手動觸發鍵 (掃描與叢發專用)
10 輸出啓用/停用鍵
11 旋鈕
12 游標鍵
13 同步接頭
14 輸出接頭

取得任一按鍵的說明

按住任何函數鍵或軟鍵以顯示該按鍵的說明主題或功能。

例如，按住 Sine 鍵：

Sine Function
Agilent 33220A 能以 1 µHz 至 20 MHz 的頻率輸出正弦曲線波形。
DONE

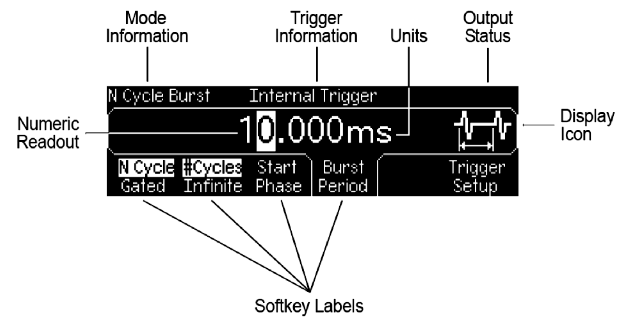
或按 Help ，以顯示「說明功能表」：

將所要的主題反白，再按 SELECT。
1 檢視最後一個顯示的訊息。
2 檢視遠端指令錯誤佇列。
SELECT CANCEL

1 Graph Mode/Local Key	**8** Waveform Selection Keys
2 On/Off Switch	**9** Manual Trigger Key (*for Sweep&Burst*)
3 Modulation/Sweep/Burst Keys	**10** Output Enable/Disable Key
4 State Storage Menu Key	**11** Knob
5 Utility Menu Key	**12** Cursor Key
6 Help Menu Key	**13** Sync Connector
7 Menu Operation Softkeys	**14** Output Connector

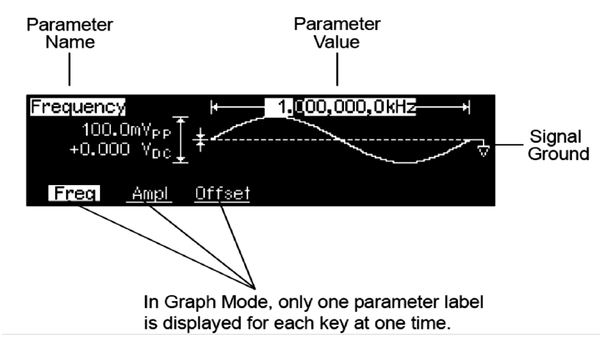
➢ FP Display

Menu Mode



Graph Mode

To enter or exit the Graph Mode, press the (Graph) *key.*



➢ Operational instruction (after power on)

➢ *Understanding:* V_{dc} ,V_m , V_p ,V_{pp} , V_{avg} , V_{rms} duty cycle, frequency/period (theory/practical), (pulse) width and edge time (rising time and falling time).

➢ A few hints

1. 發亮的按鍵表示作用中按鍵或函數，如目前作用中的波形等 (例如，Sine)。大部分的按鍵可切換開 (發亮) 或關。

2. 除非 Output 按鍵是發亮的，否則不會輸出信號。

3. 從前面板選擇 dc 電壓，按 Utility 並選取 **DC On** 軟鍵。

4. Graph 按鍵切換「圖形模式」(發亮) 和「功能表模式」。

5. 在「功能表模式」中，有六個軟鍵可讓您選取顯示器底部軟鍵功能表上的參數及函數。有些軟鍵可切換相關的參數。例如，左邊的軟鍵可在 **Freq** (頻率) 與 **Period** (週期) 之間切換，見下圖：

6. 在「圖形模式」中，除了每個按鍵只顯示一個標籤以外，軟鍵的作用與在「功能表模式」中相同。您仍然可以在相關參數間切換，如 **Freq** (頻率) 和 **Period** (週期)：

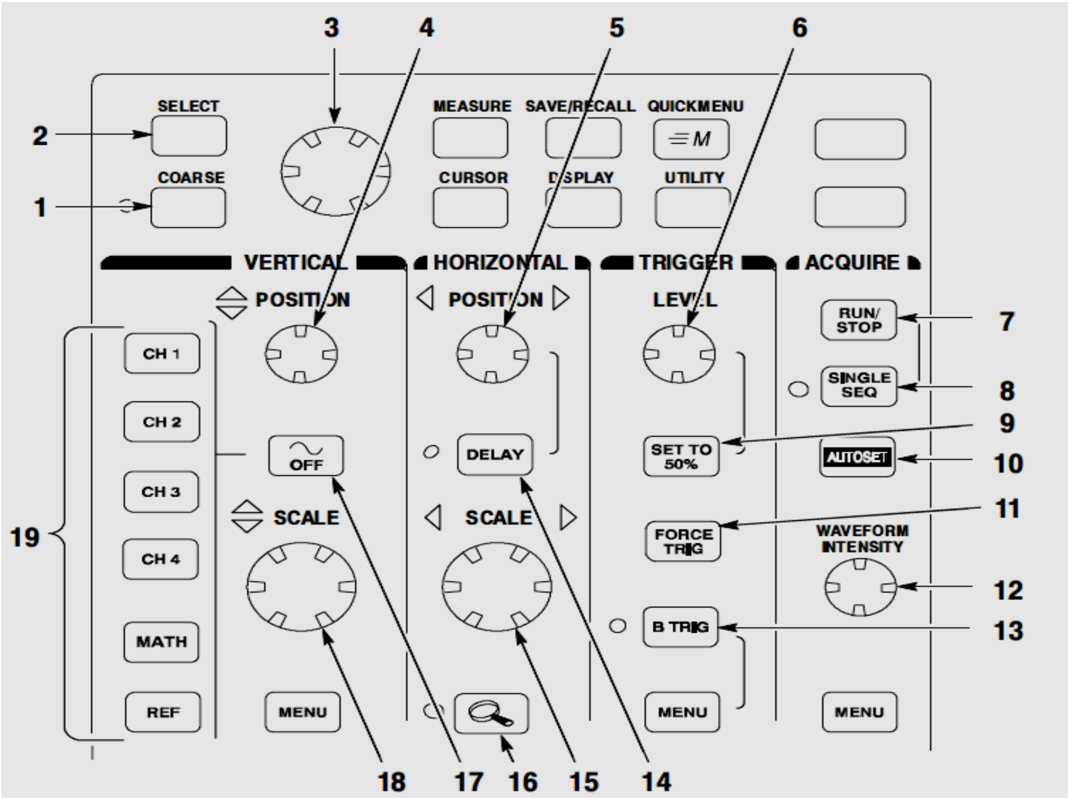
7. 你可以依振幅或偏移來指定信號，或設定其 **Hi Level** (高位準) (最大) 與 **Lo Level** (低位準) (最小) 值。請參閱《使用手冊》第 1 章，以獲得進一步資訊。

8. 調變、掃描或叢發功能可與數種類型的波形結合使用。例如，按 Square 和 Sweep ，可掃描方波。兩按鍵同時發亮，但最後按下的鍵決定顯示哪個功能表。

- **Digital Phosphor Oscilloscope (DPO) (TDS 3032)**

Tektronix 數位螢光示波器(DPO)
TDS3032 (2 channels, 300MHz bandwidth, 2.25 GS/s(Giga sample/second))

- **Front-Panel Menus and Dedicated controls**



Menus:

- MEASURE. Performs automated measurements of waveforms.
- CURSOR. Activates the cursors.
- SAVE/RECALL. Saves and recalls setups and waveforms to memory or a floppy disk.
- DISPLAY. Changes the appearance of waveforms and the display screen.
- QUICKMENU. Activates QuickMenus such as the built-in Scope QuickMenu.
- UTILITY. Activates the system utility functions, such as selecting a language.
- VERTICAL MENU. Adjusts the scale, position, and offset of waveforms. Sets the input parameters.
- TRIGGER MENU. Adjusts the trigger functions.
- ACQUIRE MENU. Sets the acquisition modes and horizontal resolution, and resets the delay time.

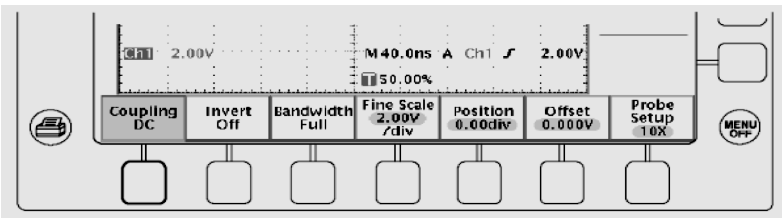
Button usages: #1 ~ #19 ~ **dedicated control** keys (without the use of menus)

1. COARSE. Causes the general purpose knob and position knobs to make adjustments more quickly.
2. **SELECT**. Toggles between the two cursors to select the active cursor.

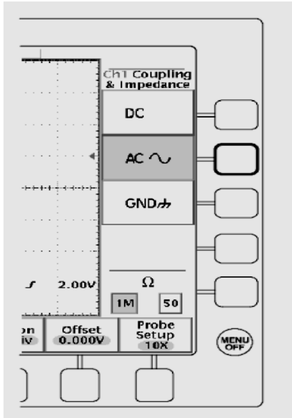
3. **General purpose knob**. Moves the cursors. Sets numerical parameter values for some menu items. Push COARSE to make adjustments quickly.
4. Vertical POSITION. Adjusts the vertical position of the selected waveform. Push COARSE to make adjustments more quickly.
5. Horizontal POSITION. Adjusts the trigger point location relative to the acquired waveforms. Push COARSE to make adjustments quickly.
6. Trigger LEVEL. Adjusts the trigger level.
7. **RUN/STOP**. Stops and restarts acquisition.
8. SINGLE SEQ. Sets acquisition, display, and trigger parameters for a single-shot (single-sequence) acquisition.
9. SET TO 50%. Sets the trigger level to the midpoint of the waveform.
10. **AUTOSET**. Automatically sets the vertical, horizontal, and trigger controls for a usable display.
11. FORCE TRIG. Forces an immediate trigger event.
12. WAVEFORM INTENSITY. Controls waveform intensity.
13. B TRIG. Activates the B trigger. Changes the trigger menu to set the B-trigger parameters.
14. DELAY. Enables delayed acquisition relative to the trigger event. Use horizontal POSITION to set the amount of delay.
15. Horizontal SCALE. Adjusts the horizontal scale factor.
16. Horizontal zoom. Splits the screen and magnifies the current acquisition horizontally.
17. Waveform OFF. Removes selected waveform from the display.
18. Vertical SCALE. Adjusts selected waveform vertical scale factor.
19. CH1, CH2 MATH. Displays a waveform and chooses the selected waveform. REF shows the reference waveform menu.

1. <u>Soft keys (Screen buttons)</u>

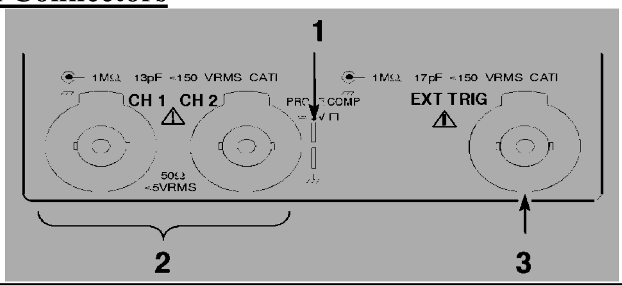
Push a bottom screen button to select a menu item. If a pop-up menu appears, continue to push the screen button to select an item from the pop-up menu.



Push a side screen button to choose a menu item. If the menu item contains more than one choice, push the side screen button again to make the choice.

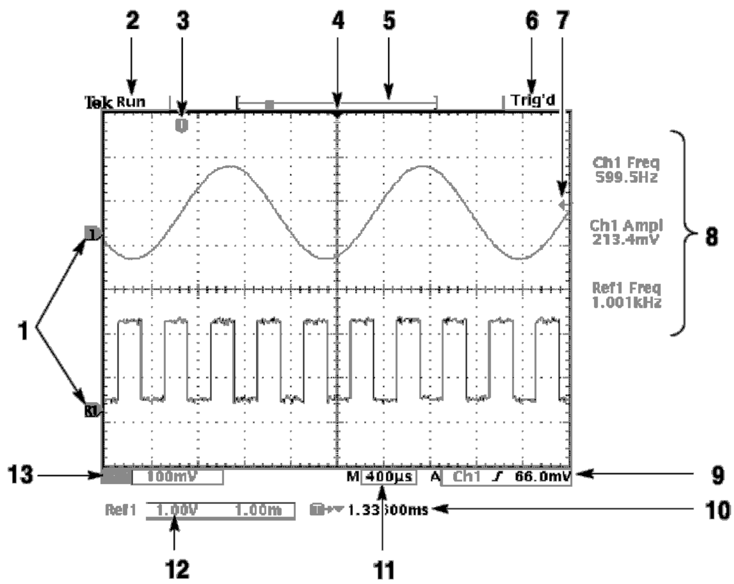


2. Front-Panel Connectors



1. **PROBE COMP**. Square wave signal source to compensate probes.
2. **CH 1, CH 2**. Channel inputs with TekProbe interface.
3. **EXT TRIG**. External trigger input with TekProbe interface (two-channel models only).

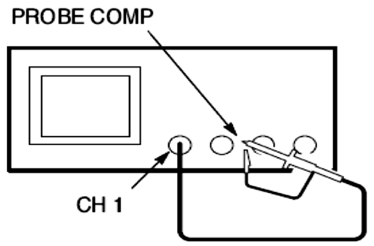
3. Identifying items on the Display (measured screen)



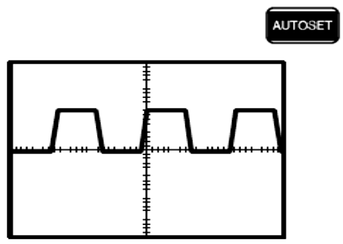
1. Waveform baseline icons show the zero-volt level of the waveforms (ignoring the effect of offset). The icon colors correspond to the waveform colors.
2. Acquisition readout shows when acquisition is in running, stopped, or when acquisition preview is in effect.
3. Trigger position icon shows the trigger location in the waveforms.
4. Expansion point icon shows the point that the horizontal scale expands and compresses around.
5. Waveform record icon shows the trigger location relative to the waveform record. The line color corresponds to the selected waveform color.
6. Trigger status readout show trigger status.
7. Trigger level icon shows the trigger level on the waveform. The icon color corresponds to the trigger source channel color.
8. **Cursor and measurement readouts** show results and messages.
9. Trigger readouts show the trigger sources, slopes, and levels, and position.
10. Readout shows the delay setting or the trigger location within the record.
11. **Horizontal readout** shows the main or zoom time/division.
12. Auxiliary waveform readouts show the vertical and horizontal scale factors of the math or reference waveforms.
13. **Channel readouts** show the channel scale factor, coupling, input resistance, bandwidth limit, and inverter

DPO Functional check and Probe compensation

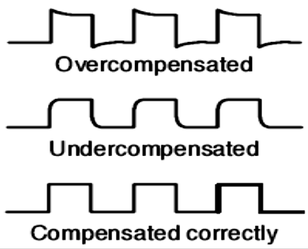
Connect the oscilloscope probe to channel 1. Attach the probe tip and reference lead to the **PROBE COMP** connectors.



Push the **AUTOSET** button. You should see a square wave in the display (approximately 5 V at 1 kHz).

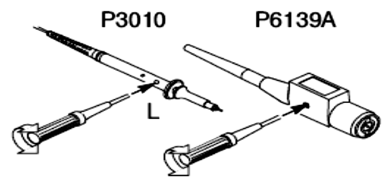


Check the shape of the displayed waveform.



*
If necessary, adjust your probe.

Repeat as necessary.



Introduction to

Logic Family, Static characteristics, and Comparisons

A. TTL (Transistor Transistor Logic) – 74/54xx series

- Standard TTL (**74**xx)
- Schottky TTL (**74S**xx)
- Low power (**74L**xx)
- Low-power Schottky TTL (**74LS**xx)
- Advanced Low-power Schottky (**74ALS**xx)
- Fast TTL (**74F**xx)

B. CMOS Family

- **4000** series(4000B) Standard CMOS (improved version)
- **40H00** series - Faster 4000 series (still slower than LS TTL
- **74C00** series – pin compatible with TTL family, slower, low-power
- **74HC00** and **74HCT00** series – high speed CMOS (~ LS TTL), TTL compatible, less power consumption. Also, **74AC** and **74ACT** series.
  → improved Advanced CMOS Technology: 74ACL/74ACT
- **74-BiCMOS** series (**74BCT**xx) – combining bipolar and CMOS transistors. Also **74BCTxx** (by TI), 74FCTxx (by Harris), and 74ABTxx (by Philip)
- **74AHC** and **74AHCT** series – one-third propagation delay, half power consumption, higher output driving currrent
- 74 low-voltage series – using 3.3V power supply
  - **LV** – Low-Voltage HCMOS
  - **LVC** – Low-Voltage CMOS
  - LVT – Low-Voltage Technology
  - **ALVC** - Low-Voltage CMOS
  - HLL – high-Speed Low-power Lower-voltage
- **74AVC** CMOS logic – advanced very low-voltage logic (1.2V ~ 3.3V)

C. ECL (Emitter-Coupled Logic) Family - for more specialized high-speed applications

- ~ TTL bipolar tech., containing a differential amp, bias circuit, and emitter follower outputs
- Much faster than TTL (74Fxx) because the transistors do not operate in saturation mode
- <u>**10K** and **100K** series</u> (shorter t_{pd} and transition time (0.7 ns), higher power consumption (40mW/gate))

D. <u>Comparisons of TTL vs CMOS family</u>

- **Dynamic timing parameters – transition and propagation time**
  - t_{PHL}, t_{PLH}, and $t_{pd} = (t_{PHL} + t_{PLH})/2$
- **Input/Output current/voltage definitions**

V_{ILmax}	The maximum voltage that an input is guaranteed to recognize as LOW.
V_{OLmax}	The maximum voltage that a LOW output is guaranteed to produce (as long as I_{OLmax} is not exceeded).
V_{IHmin}	The minimum voltage that an input is guaranteed to recognize as HIGH.
V_{OHmin}	The minimum voltage that a HIGH output is guaranteed to produce (as long as I_{OHmax} is not exceeded).
I_{ILmax}	The maximum current that an input requires to pull it LOW. Since this is a negative value, current flows *out of* the input pin.
I_{OLmax}	The maximum current that an output can supply in the LOW state while maintaining a voltage less than or equal to V_{OLmax}. Since this is a positive value, current flows *into* the output pin.
I_{IHmax}	The maximum current that an input requires to pull it HIGH. Since this is a positive value, current flows *into* the input pin.
I_{OHmax}	The maximum current that an output can supply in the HIGH state while maintaining a voltage greater than or equal to V_{OHmin}. Since this is a negative value, current flows *out of* the output pin.

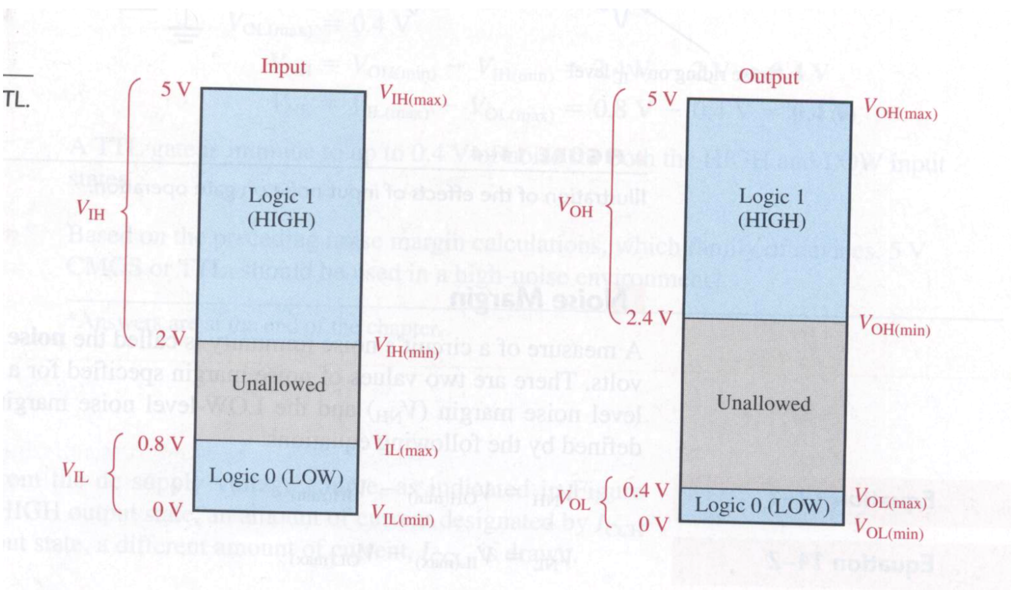


Fig. 1 I/O voltage values for TTL Tech.

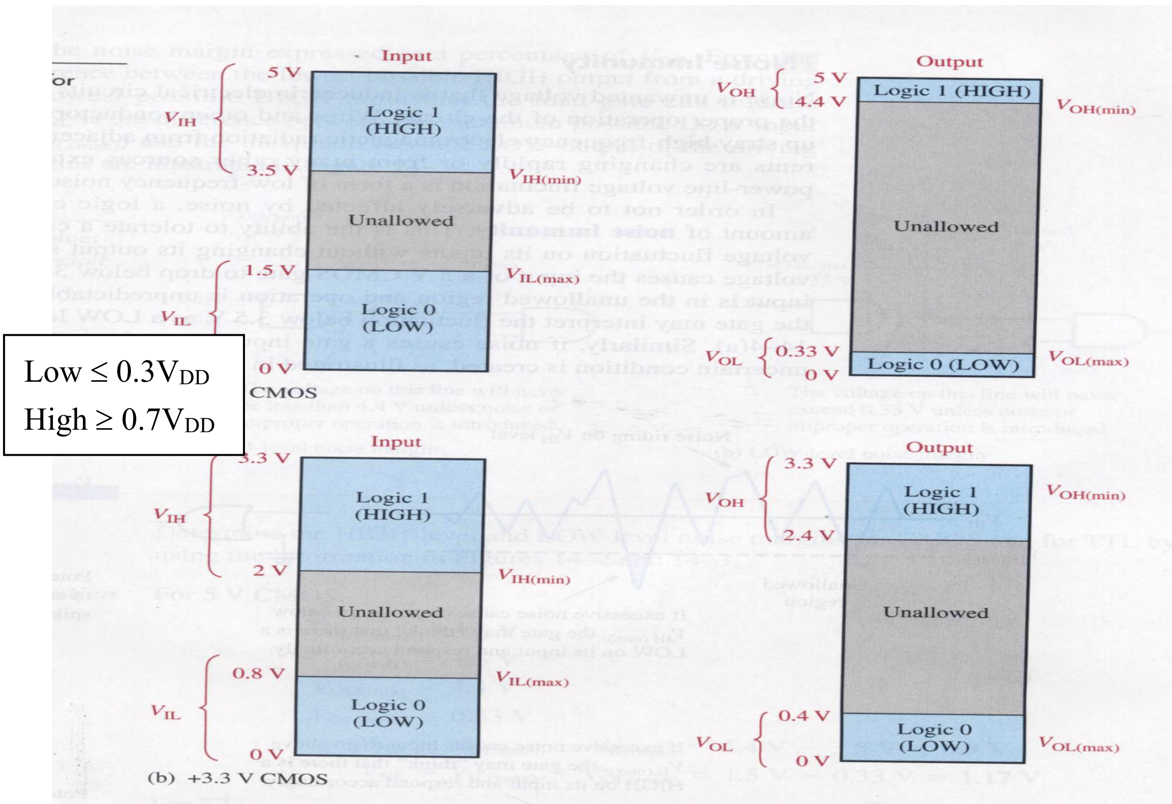


Fig. 2 I/O voltage values for CMOS Tech.

- **Noise immunity –** circuit's ability to tolerate noise at the input side
- **Noise margin –** noise immunity on logic's input

  – Quantitative measure of noise immunity or the amount of noise spike that the logic gate can withstand

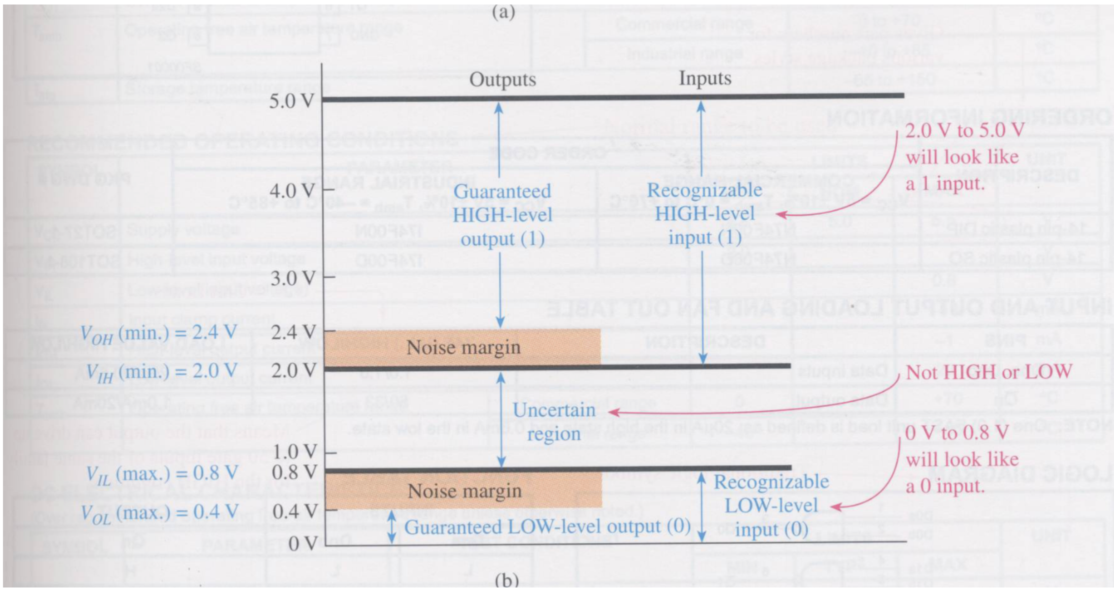


Fig. 3 NMs for TTL

NM(0) = low level NM = $V_{ILmax} - V_{OLmax}$

$= 0.8V - 0.4V = 0.4V$

NM(1) = high level NM = $V_{OHmin} - V_{IHmin}$

$= 2.4V - 2.0V = 0.4V$

- **What are the NMs for CMOS series?**

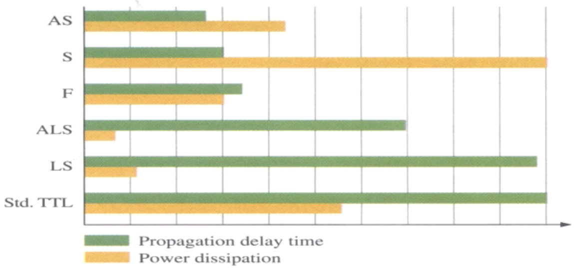
- **Power consumption/gate = (ICCH + ICCL)/2 x VCC**

- **Comparisons for TTL series**

Description	Symbol	Family 74	74L	74H	74S	74LS	74AS	74ALS
Typical propagation delay (ns)		9	33	6	3	9	1.6	5
Power consumption per gate (mW)		10	1	22	20	2	20	1.3
Speed-power product (pJ)		90	33	132	60	18	32	6.5
LOW-level input voltage (V)	V_{ILmax}	0.8	0.7	0.8	0.8	0.8	0.8	0.8
LOW-level output voltage (V)	V_{OLmax}	0.4	0.4	0.4	0.5	0.5	0.5	0.5
HIGH-level input voltage (V)	V_{IHmin}	2.0	2.0	2.0	2.0	2.0	2.0	2.0
HIGH-level output voltage (V)	V_{OHmin}	2.4	2.4	2.4	2.7	2.7	2.7	2.7
LOW-level input current (mA)	I_{ILmax}	−1.6	−0.18	−2.0	−2.0	−0.4	−2.0	−0.2
LOW-level output current (mA)	I_{OLmax}	16	3.6	20	20	8	20	8
HIGH-level input current (μA)	I_{IHmax}	40	10	50	50	20	200	20
HIGH-level output current (μA)	I_{OHmax}	−400	−200	−500	−1000	−400	−2000	−400

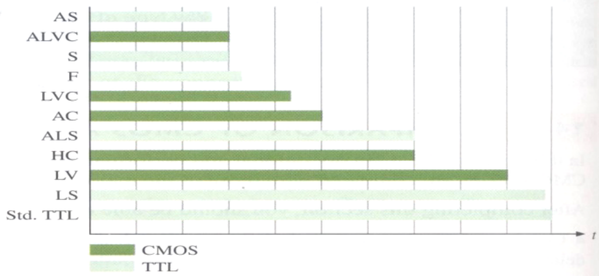
Fig. 4 TTL Characteristics comparison

◆ Timing and power comparisons for all series



▲ FIGURE 14–48

Relative comparison of propagation delay times and power dissipations within the TTL family.



▲ FIGURE 14–49

Relative comparison of propagation delay times for CMOS and TTL.

Table 14–1 provides specific parameter values of several IC logic families.

▼ TABLE 14–1

Selected performance parameters of several 74XX IC families.

	BIPOLAR (TTL)			BiCMOS	CMOS 5 V			CMOS 3.3 V		
	F	LS	ALS	ABT	HC	AC	AHC	LV	LVC	ALVC
Speed										
Gate propagation delay, t_p (ns)	3.3	10	7	3.2	7	5	3.7	9	4.3	3
FF maximum clock freq. (MHz)	145	33	45	150	50	160	170	90	100	150
Power Dissipation Per Gate										
Bipolar: 50% dc (mW)	6	2.2	1.4							
CMOS: quiescent (μW)				17	2.75	0.55	2.75	1.6	0.8	0.8
Output Drive										
I_{OL} (mA)	20	8	8	64	4	24	8	12	24	24

Fig. 5 Key parameters comparisons